



Application note

# Getting started with projects based on dual-core STM32H7 microcontrollers in STM32CubeIDE

## Introduction

This application note describes how to get started with projects based on STM32H7 Series dual-core microcontrollers in the STMicroelectronics STM32CubeIDE integrated development environment.





## 1 General information

STM32CubeIDE supports STM32 32-bit products based on the Arm<sup>®</sup> Cortex<sup>®</sup> processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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## **1.1 Prerequisites**

The following tools are prerequisites for understanding the tutorial in this document and developing an application based on the STM32H7 Series:

- STM32CubeIDE 1.4.0 or newer
- STM32Cube\_FW\_H7\_V1.7.0 or newer
- STM32CubeMX 6.0.0 or newer

Users are advised to keep updated with the documentation evolution of the STM32H7 Series at www.st.com/en/microcontrollers-microprocessors/stm32h7-series.html.

## 1.2 The use cases in this document

In the STM32CubeIDE context, users have different ways to explore and get started with the development of projects based on the STM32H7 Series. From the list below, select the description that best fits the use case considered and refer to the corresponding section in this application note:

I already have an SW4STM32 project with an ioc file:

Refer to Section 2.2 Import an SW4STM32 project with an ioc file

- I already have an SW4STM32 project without an ioc file:
- Refer to Section 2.3 Import an SW4STM32 project without an ioc file
- I want to learn with and explore example projects: Refer to Section 2.5 Import a project from the STM32CubeH7 MCU Package
- I want to start a first STM32H7 project:
  - Empty project No STM32CubeMX support for maximum flexibility.
     Refer to Section 2.4 Create an empty project based on the template in the STM32CubeH7 MCU Package
  - STM32CubeH7 project STM32CubeMX-managed project.
     Refer to Section 2.1 Create a new STM32 project

## 1.3 Specific features of dual-core microcontrollers in the STM32H7 Series

The most obvious feature of a dual-core STM32H7 device is its significant performance boost that comes from the addition of an Arm<sup>®</sup> Cortex<sup>®</sup>-M4 core besides the Arm<sup>®</sup> Cortex<sup>®</sup>-M7 core. Dual-core STM32H7 devices are also very flexible. This application note is a simple getting-started guide to get up and running with a debug session when both cores are running. It does not cover such additional features as the flexibility of being able to boot on either core or the fact that each core can exist in an independent power domain to optimize energy consumption.

## 1.3.1 Dual-core STM32H7 project structure

When a dual-core STM32H7 project is created, its structure is automatically made hierarchical. The project structure for single-core projects is flat. On the contrary, in a multi-core project, the hierarchical project structure is used. When the user creates or imports a dual-core STM32H7 project, it consists of one root project together with sub-projects, referred to as MCU projects, for each core.

The MCU projects are real CDT<sup>™</sup> projects that can contain both build and debug configurations. On the contrary, the root project is a simple container that allows sharing common code between the cores. The root project can contain neither build nor debug configurations.

If the project is not shown in a hierarchical structure, this can be changed as shown in Figure 1.

workspace - STM32CubeIDE				
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Figure 1. Setting the project hierarchical view



## 2 Create and import projects

This chapter describes how to create or import projects for dual-core microcontrollers in the STM32H7 Series.

## 2.1 Create a new STM32 project

To start a new project, go to [File]>[New]>[STM32 Project] as shown in Figure 2.

## Figure 2. New STM32 project

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Select the desired MCU or board. In the example illustrated in Figure 3, the selected board is the NUCLEO-H745ZI-Q. Click on [Next >].

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Part Number Search		~	☆ [	NUCLEO-H745ZI-Q						
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Figure 3. Target selection

After the target selection comes the project setup step shown in Figure 4. The *Targeted Project Type* setting determines whether the project gets generated by STM32CubeMX or not. An *Empty* project is a skeleton of a project that needs building upon while *STM32Cube* indicates an STM32CubeMX-managed project.

		Figure 4. Pr	ojet setup			
DE STM32 Proj	ect					×
Project Setup	)					IDE
Setup STM32	project					
Project Name:	NUCLEO-H745	5ZI-Q				
✓ Use default	location					
Location:	C:/Users/	/STM32Cu	ibeIDE/workspace	9	Bro	wse
Targeted Lan ● C ○ C++ Targeted Bin ● Executable Targeted Proc	guage ary Type le O Static Libr	ary				
	ibe O Empty					

## 2.2 Import an SW4STM32 project with an ioc file

If the project already contains an *ioc* file, the easiest way to import the project into a working STM32CubeIDE environment is to copy it and open the copy through STM32CubeMX stand alone, then, in the *Project Manager*, change the *Toolchain / IDE* to STM32CubeIDE and regenerate the project.



After the project is regenerated, go to [File]>[Import...] and choose to import it as an *Existing projects into workspace* as shown in Figure 5.

Import	-		×
Select			Ľ
Create new projects from an archive file or directory.			
Select an import wizard:			
type filter text			
🕆 🗁 General			^
🚇 Archive File			
Existing Projects into Workspace			
📮 File System			
Import ac6 System Workbench for STM32 Project			$\sim$
? < <u>B</u> ack <u>N</u> ext > <u>F</u> in	ish	Cance	

#### Figure 5. Import an existing projet with an ioc file

Then copy the code inside the different /\* USER CODE BEGIN \*/ blocks that exist in the project into the new STM32CubeIDE environment.

## 2.3 Import an SW4STM32 project without an ioc file

To make sure the project gets a hierarchical structure, the recommended way is to go to [File]>[New]>[STM32 **Project**] as shown in Figure 6.

### Figure 6. New STM32 project

IDE	workspace - S	TM32Cub	eIDE					
File	Edit Source	Refactor	Navigate	Search	Project	Run	Window Help	
	New			Alt	+Shift+N	> 🛤	Makefile Project with Existing Code	
	Open File					C	C/C++ Project	
	Open Projects	from File	System			IDE	STM32 Project	
	Recent Files		Systema			> 🖻	Project	
	Class				Ctrl IM	D++	Convert to a C/C++ Project (Adds C/C++ Nature)	
	Close				Ctri+vv	63	Source Folder	
	Close All			Ctrl+	Shift+W	<b>*</b>	Folder	
	Save				Ctrl+S	C	Source File	
	Save As					h	Header File	
B	Save All			Ctrl	+Shift+S	Ľ	File from Template	
	Revert					G	Class	
	Move					<b></b>	Other	Ctrl+N

Select the device for the project being imported and click on [Next >].



When setting up the project as shown in , make sure the *Targeted Project Type* is set to *Empty* and click on [**Finish**].

DE STM32 Project		$\times$
Project Setup		IDE
Setup STM32 project		
Project Name: NUCLEO-H745ZI-Q		
Use default location		
Location: C:/Users/ /STM32CubeIDE/workspace	Bro	wse
Options		
Targeted Language $\odot$ C $\bigcirc$ C++		
Targeted Binary Type		
• Executable		
Targeted Project Type		
O SIM32Cube O Empty		
? < <u>B</u> ack <u>N</u> ext > <u>F</u> inish	Cancel	



INUCLEO-H745ZI-Q\_Empty

Includes

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Includes

🐸 Startup

> 🐸 Inc

🕮 Src

м,

NUCLEO-H745ZI-Q Empty CM4 (in CM4)

NUCLEO-H745ZI-Q\_Empty\_CM7 (in CM7)

STM32H745ZITX FLASH.ld

STM32H745ZITX FLASH.ld

STM32H745ZITX\_RAM.ld

STM32H745ZITX\_RAM.ld

After the empty hierarchical project is generated:

- 1. Go to [File ]>[Import...]
- 2. Import the SW4STM32 project as Import ac6 System Workbench for STM32 Project
- 3. Copy and paste the project files and resources into the sub-project of the empty project as shown in Figure 8

#### Figure 8. Copy project content to empty sub-project

- ✓ NUCLEO-H745ZI-Q\_sw4stm32
  - 🔸 🕷 Binaries
  - > 🔊 Includes
  - > 🐸 CM4/Src
  - > 🐸 Common
  - > 🐸 Drivers
  - 👻 🤒 startup
    - Istartup\_stm32h745xx\_CM4.s
    - > is startup\_stm32h745xx\_CM7.s
  - > > Debug\_CM4
  - > Debug\_CM7
  - 👻 🗁 CM4
  - > 🗁 İnc
  - ✓ ➢ Src
     ☑ main.c
    - stm32h7xx\_hal\_msp.c
    - stm32h7xx\_it.c
  - 👻 🗁 CM7
    - > 🗁 Inc
    - ✓ Inc
       ✓ Inc
       ✓ Inc
       ✓ Inc
      - 🖻 main.c
      - 🖻 stm32h7xx\_hal\_msp.c
      - 🖻 stm32h7xx\_it.c
    - NUCLEO-H745ZI-Q\_sw4stm32\_Debug.hex
    - stm32h745xx\_flash\_CM4.ld
    - stm32h745xx\_flash\_CM7.ld

#### Note:

It is not recommended to import the .cproject, .project or .settings files.

It is important to remember to configure also the same build settings used previously while the project was in the SW4STM32 environment. If the project contains linked resources, these need to be updated to point to the correct resource in the file system.

This process is necessary because, when importing without any special treatment a project from SW4STM32 that does not have an *ioc* file, it is imported into STM32CubeIDE with a flat project structure.

# 2.4 Create an empty project based on the template in the STM32CubeH7 MCU Package

Follow the same steps as in Section 2.3 Import an SW4STM32 project without an ioc file but use STM32Cube\_FW\_H7 firmware in the STM32CubeH7 MCU Package as input.



## 2.5 Import a project from the STM32CubeH7 MCU Package

In order to import the STM32Cube firmware project into STM32CubeIDE, go to [File]>[Import], select *Existing Projects into Workspace* as shown in Figure 9, and click on [Next >].

### Figure 9. Import of firmware project into STM32CubeIDE

Import	 -	
Select Create new projects from an archive file or directory.		Ľ
<u>S</u> elect an import wizard:		
<ul> <li>General</li> <li>Archive File</li> <li>Existing Projects into Workspace</li> <li>File System</li> <li>Import ac6 System Workbench for STM32 Project</li> <li>Import Atollic TrueSTUDIO Project</li> </ul>		~
? < <u>Back</u> <u>Next</u> > <u>Einish</u>	(	Cancel

Then select the correct project. A project example is by default located at STM32Cube\Repository\ST
M32Cube\_FW\_H7\_VX.X.X\Projects\NUCLEO-H745ZI-Q\Examples\GPIO\GPIO\_EXTI.

### Figure 10. Firmware project selection

INDer Import			×
Import Projects		[	7
Select a directory to search for existing Eclipse projects.			
Select root directory:     C:\Users\     \STM32Cube\Repository\STM32Cube_FW_H7_V1.5.0\Projects\NUCLEO-H745ZI-Q\Examples\GPIO\GPIO_EXTI	-	B <u>r</u> owse	
O Select archive file:	·	Browse	
Projects:			
STM32H745ZI_Nucleo (C\Users\ \\STM32Cube\Repository\STM32Cube_FW_H7_V1.5.0\Projects\NUCLEO-H745ZI-Q\Examples\GPIO\GPIO_EXTI\SW4STM32\STM32H745ZI_Nucleo)	1	<u>S</u> elect A	AII
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Options Contract of the second s			
∑ search for nested projects			
Close newly imported projects upon completion			
Hide projects that already exist in the workspace			
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Wgrking sets:	S	elect	
(2)     < Back		Cancel	

After selecting the project, click on [Finish] to import and build the project.

## 3 Debugging

This chapter highlights some of the points to bear in mind while debugging a device in the STM32H7 Series. In the next two sections, this application note covers the configurations needed to start debug sessions with ST-LINK GDB server and OpenOCD.

To start configuring the launch of the debug session, right-click the sub-project (in this example, the Cortex<sup>®</sup>-M7) and select [**Debug As**]>[**Debug Configurations...**] as shown in Figure 11.

```
Figure 11. ST-LINK GDB server debug configuration (1 of 6) and OpenOCD debug configuration (1 of 3)
```





For the rest of this section, examples are based on the NUCLEO-H755ZI-Q board.

## 3.1 Setting up with ST-LINK GDB server

Since the STM32CubeMX default project puts the Cortex<sup>®</sup>-M4 in the Deepsleep mode, the **[Reset behaviour]** field must be set to *Connect under reset* to be able to communicate with the CPU (refer to Figure 12). The *Halt all cores* option must not be set. Setting it prevents the Cortex<sup>®</sup>-M4 from starting to execute the code. The Cortex<sup>®</sup>-M4 must execute the code and go to Stop mode before the Cortex<sup>®</sup>-M7 can start executing the code and wake up the Cortex<sup>®</sup>-M4 by releasing a hardware semaphore. In the debug configuration, select *Enable shared ST-LINK*, switch to the *Startup* tab and select [**Add...**].

Debug Configurations		– 🗆 X
Create, manage, and run configurations		Ť.
Create, manage, and run configurations	Name       NUCLEO-H745ZI-Q_CM7 Debug            Main	sst
	Misc Verify flash download Enable live expressions C:\Users\burguera\STM32CubelDE\worf External Loader: Shared ST-LINK Max halt timeout(s): 2	kspace_1.9.0.22w04\NUCLEO-H745ZI-Q\CM7\Debug\st-I Browse Scan Initialize
		<u>D</u> ebug Close

#### Figure 12. ST-LINK GDB server debug configuration (2 of 6)



## Startup tab - Cortex<sup>®</sup>-M7

The Cortex<sup>®</sup>-M7 debug configuration is responsible for loading both the Cortex<sup>®</sup>-M7 and Cortex<sup>®</sup>-M4 images. Go to the *Startup* tab to do this as shown in Figure 13:

	5 0	,	,						
Debug Configurations									
Create, manage, and run configuration	ins				Ś				
🗋 🖻 🗫 🖪 🗮 🗖	Name: NUCLEO-H755-O_CM7 Debug								
type filter text	Main      Pobugger      Startup      Source □ Common								
C/C++ Application	Initialization Commands								
C/C++ Postmortem Debugger					^				
C/C++ Remote Application					×				
<ul> <li>GDB Hardware Debugging</li> <li>Launch Group</li> <li>Launch Group (Deprecated)</li> </ul>	Load Image and Symbols								
	File Debua/NUCLEO-H755-O CM4.elf [NUCLEO-H755-O CM4]	Load sy true	Add						
<ul> <li>STM32 Cortex-M C/C++ Application</li> <li>NUCLEO-H755-Q_CM4 Debug</li> <li>NUCLEO-H755-Q_CM7 Debug</li> </ul>	► Debug\NUCLEO-H755-Q_CM7.elf [NUCLEO-H755-Q_CM7]	See Main	🖋 true	<ul> <li>v true</li> <li>✓ true</li> </ul>	Edit				
					Remove				
					Move up				
					Move down				
	Runtime Options								
	Set program counter at (hex):								
	Set breakpoint at: main								
	Exception on divide by zero								
	Halt on exception								
	✓ Resume								
	Run Commands								
				t	Anal				
Filter matched 10 of 10 items			Ke	vert	Арріу				
(٢)			<u>D</u> e	bug	Close				

#### Figure 13. ST-LINK GDB server debug configuration (3 of 6)

To download also the  $Cortex^{\ensuremath{\mathbb{B}}}$ -M4 image, click [**Add...**], browse the correct project, and build the configuration. The result is shown in Figure 14.

Figure 14. ST-LINK GDB	server debug	configuration	(4	of 6)	)
------------------------	--------------	---------------	----	-------	---

DE Add/Edit item				×	
This file is already us	ed.				
Project:	NUCLEO-H	755-Q	_CM4	~	
Build configuration:	Debug			~	
Program path:	Debug/NU	CLEO-	H755-Q	_CM4.elf	
	File system				
🗹 Perform build					
🗹 Download					
Use download offs	et (hex)				
✓ Load symbols					
Use symbol address (hex)					
	OK		Can	cel	

The order in the load list is very important. The last entry in the list, marked by a green arrow (refer to Figure 13, is the image debugged with this debug configuration. Consequently, the debugger fetches the program counter value (PC) from this image.



## Startup tab - Cortex<sup>®</sup>-M4

As shown in Figure 15:

- Make sure that the *Port number* exceeds the value of the previous debug configuration by at least 3 (61238 in this example)
- Select 3 Cortex-M4 for [Access port]
- Select None for [Reset behaviour]
- Select Enable shared ST-LINK

## Figure 15. ST-LINK GDB server debug configuration (5 of 6)

Debug Configurations	— 🗆 X
Create, manage, and run configuration	ns 🐞
	1
Image: Second secon	Name:       NUCLEO-H755-Q_CM4 Debug         Image:       Main       Debugger         Startup       Source       Common         GDB Connection Settings       Image: Common Settings         Image:       Autostart local GDB server       Host name or IP address         Image:       Image: Common Setting Server       Image: Common Setting Server
<ul> <li>C/C++ Remote Application</li> <li>GDB Hardware Debugging</li> <li>Launch Group</li> <li>Launch Group (Deprecated)</li> <li>STM32 Cortex-M C/C++ Application</li> <li>NUCLEO-H755-Q_CM4 Debug</li> <li>NUCLEO-H755-Q_CM7 Debug</li> </ul>	O Connect to remote GDB server Port number 61238 Debug probe ST-LINK (ST-LINK GDB server) → GDB Server Command Line Options Interface
	Image: SWD       JIAG       Use specific S1-LINK S/N       Image: Scan         Access port:       3 - Cortex-M4       Image: Scan         Reset behaviour       Image: Scan       Image: Scan         Type:       None       Image: Hait all cores
	Serial Wire Viewer (SWV)  Enable  Clock Settings  Core Clock: 16.0 MHz  SWO Clock: 2000 KHz  Port number: 61235  Wait for sync packet
	Cross Trigger Interface (CTI) Allow other cores to halt this core Signal halt events to other cores Misc Verify flash download Signal Live expressions
	Log to file:       C:\Users\ \STM32CubeIDE\workspace\NUCLEO-H755-Q\CM4\Debug} Browse         External Loader:       Scan         Enable shared ST-LINK
Filter matched 10 of 10 items	Re <u>v</u> ert Apply
0	<u>D</u> ebug Close

Go to the *Startup* tab and select [**Edit...**]>[**Disable Download**]. This is required since the download is already performed by the Cortex<sup>®</sup>-M7 configuration (refer to Figure 16).

Create, manage, and run configurations         Create, manage, and run configurations         Image: Statup         Imade: Statup         <	Image angunation       Image and provide the set of the set	Debug Configurations		- П X
Create, manage, and run configurations	Create, manage, and run configurations         Image: Im			-
Image: NUCLEO-H755-Q_CM4 Debug   Type filter text   C/C++ Application   C/C++ Application   C/C++ Remote Application   C/C++ Remote Application   C/C++ Remote Application   C/C++ Application   STM32 Cortex-M C/C++ Application   Image and Symbols   File   Debug\NUCLEO-H755-Q_CM4 Debug   NUCLEO-H755-Q_CM7 Debug   Move up   Move up   Move down   Runtime Options   Set program counter at (hex):   Set breakpoint at:   Set program counter at (hex):   Set breakpoint at:   Main   Everption on divide by zero   Exception on unaligned access   Halt on exception   Renore   Run Commands	type filter text   © (C++ Application   © (C++ Application   © (C++ Pernote Application   © (C++ Remote Application   © GOB Hardware Debugger   © IMAD Concert   IMAD Concert   © IMAD Concert	Create, manage, and run configuration	ons	) Or
Image: Startup   Image: NUCLEO-H755-Q_CM4 Debug   Image: NUCLEO-H755-Q_CM7 Debug   Image: NUCL	Image: Statup       Statup       Source       Common         Image: C/C++ Application       Image: Statup       Source       C/C++ Application         Image: Source Application       Image: Statup       Source       C/C++ Application         Image: Source Application       Image: Statup       Source       Mode         Image: Source Application       Image: Source Application       Image: Source       Add         Image: Source Application       Image: Source Application       Image: Source Application       Image: Source Application         Image: Source Application       Image: Source Application       Image: Source Application       Image: Source Application       Image: Source Application         Image: Source Application       Image: Source Application       Image: Source Application       Image: Source Application       Image: Source Application         Image: Source Application       Image: Source Application       Image: Source Application       Image: S			
type filter text     C/C++ Application   C/C++ Postmortem Debugger   C/C++ Postmortem Debugger   C/C++ Remote Application   C/C++ Remote Application   GDB Hardware Debugging   Launch Group   Launch Group (Deprecated)   *   StM32 Cortex-M C/C++ Application   NUCLEO-H755-Q_CM4 Debug   Remove   Move up   Move down   Runtime Options   Set program counter at (hex):   Hat on exception on unaligned access   Hat on exception   Remove   Run Commands	type filte text     © C(++ Atach to Application   © C(++ Atach to Application   © C(++ Remote Application   © C(++ Remote Application   © C(++ Remote Application   © DB Hardware Debugging   © Lauch Group   > Lauch Group (Deprecated)   © NUCLEO+H755-Q_CM7 Debug     File   DebugNUCLEO+H755-Q_CM7 Debug     Runtime Options   © Exception on divide by zero   © Exception on divide by zero   © Resume   Run Commands		Name: NUCLEO-H755-Q_CM4 Debug	
<ul> <li>C/C++ Application</li> <li>C/C++ Attach to Application</li> <li>C/C++ Remote Application</li> <li>G/C++ Remote Application</li> <li>STM32 Cortex-M C/C++ Application</li> <li>SUCLEO-H755-Q_CM4 Debug</li> <li>NUCLEO-H755-Q_CM7 Debug</li> <li>NUCLEO-H755-Q_CM7 Debug</li> <li>Remove</li> <li>Move up</li> <li>Move down</li> <li>Runtime Options</li> <li>Set program counter at (hex):</li> <li>Set breakpoint at:</li> <li>Main</li> <li>Exception on divide by zero</li> <li>Exception on unaligned access</li> <li>Halt on exception</li> <li>Resume</li> <li>Run Commands</li> </ul>	C/C++ Abplication C/C++ AbotA to Application C/C++ Postmortem Debugger C/C++ Abplication C/C++ Remote Application C/C++ Remote Application C/C++ Applicatio	type filter text	■ Main 参 Debugger ▶ Startup 与 Source □ <u>C</u> ommon	
<ul> <li>□ C/C++ Postmottem Debugger</li> <li>□ C/C++ Postmottem Debugging</li> <li>■ Launch Group</li> <li>□ Launch Group (Deprecated)</li> <li>~ □ STM32 Cortex-M C/C++ Application</li> <li>□ NUCLEO-H755-Q_CM4 Debug</li> <li>□ NUCLEO-H755-Q_CM7 Debug</li> <li>□ NUCLEO-H755-Q_CM7 Debug</li> <li>□ Remove</li> <li>□ Move down</li> <li>Remove</li> <li>□ Move down</li> <li>Runtime Options</li> <li>□ Set program counter at (hex):</li> <li>□ Resume</li> <li>Run Commands</li> </ul>	Cyc++ Postimortem Debugger       Cyc++ Postimortem Debugger         Cyc++ Remote Application       Image and Symbols         Istanch Group       Istanch Group (Deprecated)         STM32 Cortex-M Cyc++ Application       File         NUCLEO-H755-Q_CM7 Debug       Debug(NUCLEO-H755-Q_CM4.eff [NUC See Main)         Image and Symbols       Edit         Remove       Move ub         Move down       Move down         Runtime Options       Set program counter at (her):         Set brackpoint at:       main         Exception on unaligned access       Halt on exception         Resume       Resume         Ron Commands       Image and set mediate access	C/C++ Application	Initialization Commands	
© C/C++ Remote Application © GDB Hardware Debugging @ Launch Group Launch Group Launch Group (Deprecated) > © STM32 Cortex-M C/C++ Application © NUCLEO-H755-Q_CM4 Debug © NUCLEO-H755-Q_CM4 Debug © NUCLEO-H755-Q_CM7 Debug © NUCLEO-H755-Q_CM7 Debug Remove Move up Move up Move down Runtime Options Set program counter at (hex): Set breakpoint at: Set program counter at (hex): Set breakpoint at: Main Set program counter at (hex): Set breakpoint at: Main Main Runtime Options Set program counter at (hex): Remove Halt on exception Run Commands Run Commands Run Commands	C(C/+ + Renote Application     GDB Hardware Debugging     Launch Group     Launch Group (Deprecated)     STM32 Cortee: M C/C+ + Application     MOUCLEO-H755-Q_CM4 Debug     NUCLEO-H755-Q_CM7 Debug     Move down     Runtime Options     Set program counter at (hex):     Set broskpoint at:     Main     Move down     Runtime Options     Set broskpoint at:     Main     Move down     Runtime Options     Set program counter at (hex):     Stereption on unaligned access     Halt on exception     Resume     Run Commands     Run Commands     Success	C/C++ Postmortem Debugger		~
Load Image and Symbols  Load Image and Symbols  Load Image and Symbols  File Debug\NUCLEO-H755-Q_CM4.Debug NUCLEO-H755-Q_CM4.Debug NUCLEO-H755-Q_CM7 Debug NUCLEO-H755-Q_CM7 Debug Runtime Options Set program counter at (hex): Set breakpoint at: Set program counter at (hex): Se	Lad Image and Symbols  Launch Group Launch Group Launch Group MUCLEO-H755-Q_CMA Debug  NUCLEO-H755-Q_CMA Debug NUCLEO-H755-Q_CMA Debug NUCLEO-H755-Q_CMA Debug NUCLEO-H755-Q_CMA Debug NUCLEO-H755-Q_CMA Debug NUCLEO-H755-Q_CMA Debug Nucceotion	C/C++ Remote Application		×
<ul> <li>Launch Group (Deprecated)</li> <li>STM32 Cortex-M C/C++ Application</li> <li>NUCLEO-H755-Q_CM4 Debug</li> <li>NUCLEO-H755-Q_CM7 Debug</li> <li>Remove</li> <li>Move up</li> <li>Move up</li> <li>Move down</li> <li>Runtime Options</li> <li>Set program counter at (hex):</li> <li>Set breakpoint at:</li> <li>Main</li> <li>Exception on unaligned access</li> <li>Halt on exception</li> <li>Resume</li> <li>Run Commands</li> </ul>	Launch Group (Deprecated) Launch Group (Deprecated) Debug\NUCLEO-H755-Q_CM4 elf [NUC See Main • false • true Editt Remove Move down Runtime Options Set program counter at (hex): Set breakpoint at: Main Exception on divide by zero Exception on divide by zero Exception on divide by zero Runtomedia access Halt on exception Run Commands Commands Output	<ul> <li>GDB Hardware Debugging</li> <li>Launch Group</li> </ul>	Load Image and Symbols	
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Resume Run Commands	Resume		Halt on exception	
Run Commands	Run Commands		Resume	
			Run Commands	
				^
				×
Filter matched 10 of 10 items Revert Apply	ilter matched 10 of 10 items Revert Apply	Filter matched 10 of 10 items	Re <u>v</u> ert	Apply
	② Debug Close	?	Debug	Close

## Figure 16. ST-LINK GDB server debug configuration (6 of 6)

The configuration is complete.



#### 3.1.1 Launching the configurations

- 1. Launch the Cortex<sup>®</sup>-M7 configuration to download both the Cortex<sup>®</sup>-M4 and Cortex<sup>®</sup>-M7 images
- Set the Cortex<sup>®</sup>-M7 core running so that the HSEM semaphore is released and Cortex<sup>®</sup>-M4 wakes up from Stop mode
- Launch the Cortex<sup>®</sup>-M4 configuration using the arrow next to the debug icon. It is in the running mode and the user can halt it.

#### Figure 17. ST-LINK GDB server debug configuration launch



Note: After creating the debug configurations for both cores, they are not shown in the scroll-down menu if they have never been launched before. This is because the arrow provides access to the history of latest launches, with a grayed "no history" message if there are none. First-time degug launch must be done through the debug configuration wizard.

When debugging an STM32H7 device with the ST-LINK GDB server, it is possible to create a launch group, which offers the following advantages:

 The user can launch the debug session on both cores with only one launch configuration as shown in Figure 18.



#### Figure 18. ST-LINK GDB server launch group

The user can stop both cores using the launch group. This avoids having to terminate both debug sessions individually.



## 3.1.2 Cross-trigger Interface

The cross-trigger interface is used to send halt signals from one core to the other. To enable the Cortex<sup>®</sup>-M4 to halt the Cortex<sup>®</sup>-M7, apply the following configuration:

- In the Cortex<sup>®</sup>-M4 debug configuration: select Signal halt events to other cores
- In the Cortex<sup>®</sup>-M7 debug configuration: select Allow other cores to halt this core

#### Figure 19. ST-LINK GDB server debug cross-trigger interface

Cross Trigger Interface (CTI)
Allow other cores to halt this core Signal halt events to other cores

Note: Checking both checkboxes in both debug configurations enables both cores to halt each other.



3.2

## Setting up with OpenOCD

Select *ST-LINK (OpenOCD)* as the [**Debug probe**]. Select *Autostart local GDB server* for the configuration that launches first, which is the Cortex<sup>®</sup>-M7 in the example in Figure 20. Set all the default options and verify that:

- Connect under reset is selected as [Reset Mode].
- [Shared ST-LINK] is selected; this option is mandatory to run the multicore target.

## Figure 20. OpenOCD debug configuration (2 of 3)

Debug Configurations		– 🗆 X
Create, manage, and run configurations		The second secon
🗋 🖻 🐌 🗎 🗮 🖻 🌩 🗸	Name: NUCLEO-H755-Q_CM7 Debug OpenOCD	]
type filter text	📄 Main 🏂 Debugger 🍉 Startup 🤴 Source 🔲 <u>C</u> ommon	
C //C++       Application         C //C++       Attach to Application         C //C++       Remote Application         L aunch Group       L aunch Group (Deprecated)         ✓ Ims       NUCLEO-H755-O_CM4 Debug Oper         M NUCLEO-H755-O_CM7 Debug Oper       NUCLEO-H755-O_CM7 Debug Oper	Wath y Debugger y Survey yourse	Hide generator options Browse Reload ander reset power modes ters when halt
< > Filter matched 10 of 10 items		Reyert Apply
0		



Create the debug configuration for the other core, which is the Cortex<sup>®</sup>-M4 in the example in Figure 21:

- Select ST-LINK (OpenOCD) as the [Debug probe]
- Select Autostart local GDB server as default
- Make sure that the *Port number* exceeds the value of the previous debug configuration by at least 2 (3335 in this example)
- Open [Generator Options] and select Core reset as [Reset Mode]

#### Figure 21. OpenOCD debug configuration (3 of 3)

Debug Configurations	- C	) X
Create, manage, and run configurations		the
🖹 🖻 🖚 🗎 🗶 🗐 🎝 🔻	Name: NUCLEO-H755-Q_CM4 Debug OpenOCD	
type filter text	Main 🕸 Debugger 🔈 Startup 🤴 Source 🔲 Common	
type filter text         © C/C++ Application         © C/C++ Attach to Application         © C/C++ Remote Application         © GDB Hardware Debugging         ■ Launch Group         ▶ Launch Group (Deprecated)         ▼ 100 STM32 Cortex-M C/C++ Application         101 NUCLEO-H755-Q_CM4 Debug Opei         101 NUCLEO-H755-Q_CM7 Debug Opei	Mini %> Debugger IP Startup % Source ☐ common         GDB Connection Settings         Image: Autostart local GDB server         Pot number         3335         Debug probe         ST-LINK (OpenOCD)         GDB Server Command Line Options         OpenOCD Stup         OpenOCD Stup         OpenOCD Stup         OpenOCD Options :         Configuration Script         Image: Automated Generation         Outper Defined         File:         Script File:         SpenCD Options:         Connection Setup         Interface:         Swid         Frequency:         BMHz         Frequency:         BMHz         Constring Stript File:         Stop watchdog counters when halt            Cross Trigger Interface (CTI)           Allow other cores to halt this core            Stards ST-LINK            Boards detected by ST-Link Server: 1            Name            Stards Stigstigstigstigstigstigstigstigstigstigs	
<		
Filter matched 10 of 10 items	Reyert Ap	pl <u>v</u>
?	<u>D</u> ebug C	Close

The configuration of the *Startup* tab is the same as with the ST-LINK GDB server probe for both debug configurations (refer to Startup tab - Cortex-M7 and Startup tab - Cortex-M4 in Section 3.1 Setting up with ST-LINK GDB server).

## 3.2.1 Launching the configurations

After both debug configurations are set up, save them and click on the arrow next to the debug icon to make sure launching the autostarting local GDB server first (the Cortex<sup>®</sup>-M7 in this example). After this first launch, click on the same arrow again and launch the other configuration.

### Figure 22. OpenOCD debug configuration launch

• 🖄 🛷 🕶 🗾 🔛 🗐 🖷 🐕 🕶 🖓 🕶 🍫 🔶	•
1 NUCLEO-H755-Q_CM4 Debug OpenOCD	
2 NUCLEO-H755-Q_CM7 Debug OpenOCD	
3 New_configuration	
Debug As	>
Debug Configurations	
Organize Favorites	
	Image: Second Secon

Note: After creating the debug configurations for both cores, they are not shown in the scroll-down menu if they have never been launched before. This is because the arrow provides access to the history of latest launches, with a grayed "no history" message if there are none. First-time degug launch must be done through the debug configuration wizard.

When debugging an STM32H7 device with OpenOCD, it is possible to create a launch group, which offers the following advantages:

The user can launch the debug session on both cores with only one launch configuration.

Debug Configurations		-	100	
Create, manage, and run configurati Launch several other configurations sequ	ons entially			Ť.
□ 🖻 🖗 🗎 🗶 📄 🕇 🗸	Name: Launch H757			
type filter text	🗸 Launches 🔲 Common			
C/C++ Application	Name	Mode	Action	Up
C C/C++ Attach to Application	♥ DE STM32 Cortex-M C/C++ Application::H757_CM7 Debug ♥ DE STM32 Cortex-M C/C++ Application::H757_CM4 Debug	Inherit Inherit		Down
C GDB Hardware Debugging				Edit
Launch H757				Add
Launch Group (Deprecated) STM32 Cortex-M C/C++ Applicat				Remove
ITST_CMU Debug	<		4	
	< III.			۱.
Filter matched 11 of 11 items			Revert	Apply
?			Debug	Close

#### Figure 23. Launch OpenOCD debug on both cores

• The user can stop both cores using the launch group. This avoids having to manually terminate both debug sessions individually. In Figure 24, the launch group in pink handles each of the cores in green.



#### Figure 24. Stop OpenOCD debug on both cores

## 3.2.2 Cross-trigger interface

The cross-trigger interface is used to send halt signals from one core to the other. To enable the Cortex<sup>®</sup>-M4 to halt the Cortex<sup>®</sup>-M7, apply the following configuration:

- In the Cortex<sup>®</sup>-M4 debug configuration: select Signal halt events to other cores
- In the Cortex®-M7 debug configuration: select Allow other cores to halt this core

#### Figure 25. OpenOCD debug cross-trigger interface

	Cross Trigger Interface (CTI)	
Allow other cores to halt this core Signal halt events to other cores	Allow other cores to halt this core Signal halt events to other cores	

Note: Checking both checkboxes in both debug configurations enables both cores to halt each other.

## **Revision history**

## Table 1. Document revision history

Date	Revision	Changes
21-Nov-2019	1	Initial release.
23-Jul-2020	2	<ul> <li>Reorganized Section 3 Debugging:</li> <li>Updated Section 3.1 Setting up with ST-LINK GDB server, Section 3.1.1 Launching the configurations, and added Figure 18. STLINK GDB server launch group</li> <li>Updated Section 3.2 Setting up with OpenOCD, Figure 20. OpenOCD debug configuration (2 of 3), Figure 21. OpenOCD debug configuration (3 of 3) and Section 3.2.2 Cross-trigger interface</li> </ul>
10-Jun-2021	3	Updated Figure 11 in Section 3 Debugging.
9-Feb-2022	4	Updated the Figure 12 and its introduction in Section 3.1 Setting up with ST-LINK GDB server.

## Contents

1	Gen	eral infe	ormation	2
	1.1	Prerec	quisites	2
	1.2	The us	se cases in this document	2
	1.3	Specif	fic features of dual-core microcontrollers in the STM32H7 Series	2
		1.3.1	Dual-core STM32H7 project structure	2
2	Crea	ate and	import projects	4
	2.1	Create	e a new STM32 project	4
	2.2	Import	t an SW4STM32 project with an ioc file	6
	2.3	Import	t an SW4STM32 project without an ioc file	7
	2.4	Create	e an empty project based on the template in the STM32CubeH7 MCU Packa	age9
	2.5	Import	t a project from the STM32CubeH7 MCU Package	10
3	Deb	ugging		
	3.1	Setting	g up with ST-LINK GDB server	12
		3.1.1	Launching the configurations	17
		3.1.2	Cross-trigger Interface	18
	3.2	Setting	g up with OpenOCD	19
		3.2.1	Launching the configurations	21
		3.2.2	Cross-trigger interface.	22
Rev	vision	history	,	23
List	of fig	jures		

# List of figures

Figure 1.	Setting the project hierarchical view.	3
Figure 2.	New STM32 project.	4
Figure 3.	Target selection	5
Figure 4.	Projet setup	6
Figure 5.	Import an existing projet with an ioc file	7
Figure 6.	New STM32 project.	7
Figure 7.	Projet setup	8
Figure 8.	Copy project content to empty sub-project	9
Figure 9.	Import of firmware project into STM32CubeIDE	0
Figure 10.	Firmware project selection	0
Figure 11.	ST-LINK GDB server debug configuration (1 of 6) and OpenOCD debug configuration (1 of 3) 1	1
Figure 12.	ST-LINK GDB server debug configuration (2 of 6) 1	2
Figure 13.	ST-LINK GDB server debug configuration (3 of 6)	3
Figure 14.	ST-LINK GDB server debug configuration (4 of 6)	4
Figure 15.	ST-LINK GDB server debug configuration (5 of 6)	5
Figure 16.	ST-LINK GDB server debug configuration (6 of 6)	6
Figure 17.	ST-LINK GDB server debug configuration launch 1	7
Figure 18.	ST-LINK GDB server launch group	7
Figure 19.	ST-LINK GDB server debug cross-trigger interface	8
Figure 20.	OpenOCD debug configuration (2 of 3)	9
Figure 21.	OpenOCD debug configuration (3 of 3)	0
Figure 22.	OpenOCD debug configuration launch	1
Figure 23.	Launch OpenOCD debug on both cores	1
Figure 24.	Stop OpenOCD debug on both cores 2	2
Figure 25.	OpenOCD debug cross-trigger interface 2	2

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